V.L.S.I. Lab Report (Tanner)

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Tezpur University

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CONTENT

Assignment 1: Active Load NMOS

Using an active load NMOS, to replace a passive load resistor can dramatically reduced the required chip area for the circuit while also helping produce much higher gains (due to the potentially high small-signal resistance an active load can provide). An active load can be implemented using a gate-drain connected (a.k.a. diode-connected) MOSFET or a current source/sink. Amplifiers with gate-drain connected active loads tend to achieve large frequency bandwidths but low gain due to their relatively low output impedance. For examples of NMOS amplifiers using gate connected active loads is shown in circuit diagram below.

The input to the inverter is at the gate of the N-channel output transistor and $V_{IN} = V_{GS}$. The output is at the drain and

$$\mathbf{V_{OUT} = V_{DS} = V_{DD} - I_{RL}.}$$

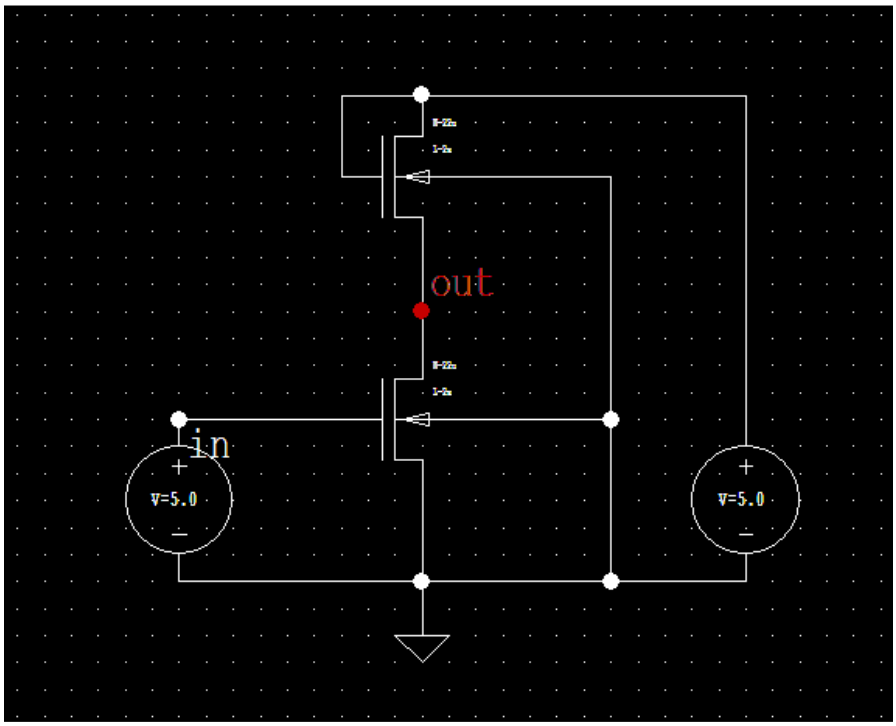
For $V_{IN} < V_t$ is cut off and does not conduct drain current. Since the resistor current is equal to the drain current, with V_{IN} V_t I = I_D(OFF) = 0 and the output is

$$\mathbf{V_{OUT} = V_{DD}.}$$

As the input is increased slightly above the threshold voltage begins to conduct. At this point only a small current flows and the drain voltage is lightly less than V_{DD}. As long as $V_{DS} >= V_{GS} - V_t$ is operating in the saturation region. With further increase of the input, a larger drain current conducts and the output voltage continues to fall. In summary, for a low input the output is high. Conversely for a high input the output is low. In a depletion-mode NMOS the channel area is doped so that the channel exists even with no (positive) applied V_{GS}. Thus, the threshold of a depletion-mode is typically negative. The short-circuit between Gate and Source (i.e. V_{GS}=0) ensures that the transistor is always ON since

$$\mathbf{V_T<0, V_{GS}=0,}$$
$$\mathbf{-V_T>0, V_{GS}=0,}$$
$$\mathbf{V_{GS}-V_T>0.}$$

Circuit Diagram:



Netlist Codes:

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* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on April 23, 2010 at 22:52:21
* Waveform probing commands
.probe
.options probefilename="File0.dat"
+ probesdbfile="File0.sdb"
+ probetopmodule="Module0"
* Main circuit: Module0
 M1 N11 N11 out Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u
 M2 out in Gnd Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u
 v3 in Gnd 5.0
 v4 N11 Gnd 5.0
```

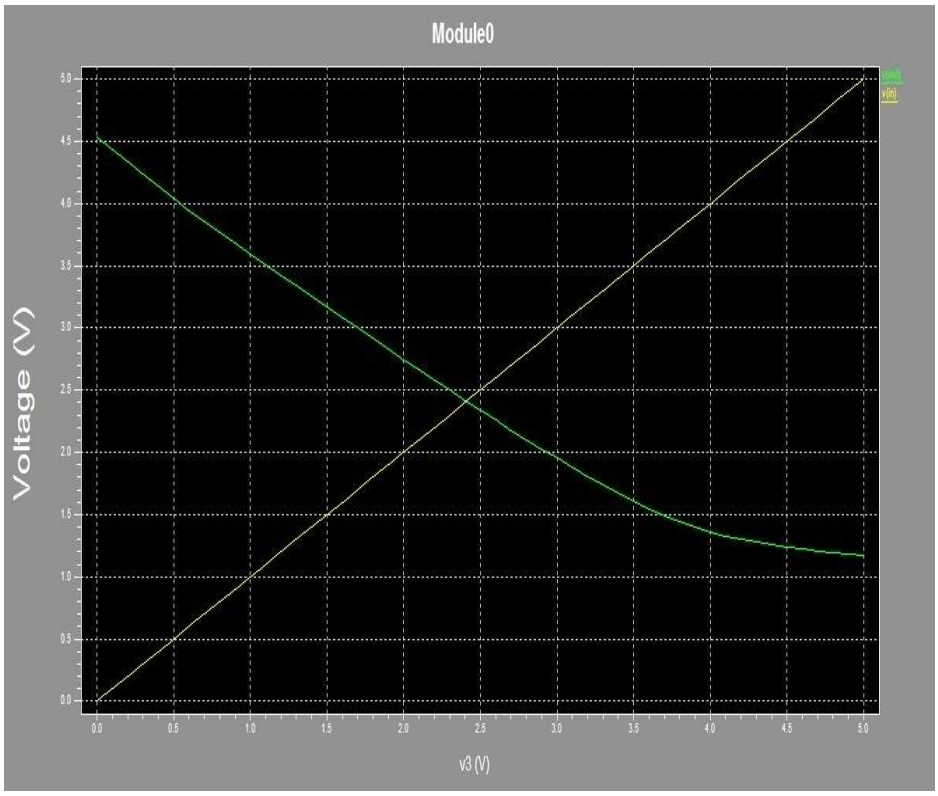
.include "D:\Tanner\Model file\dual.md"

.dc v3 0 5 .1

.print v(in) v(out)

* End of main circuit: Module0

Characteristic Graph:

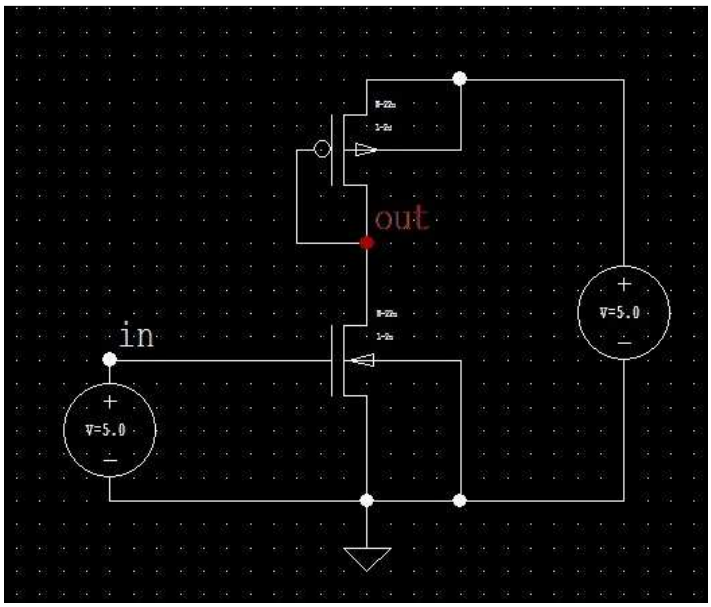


Assignment 2: Active load PMOS

The active PMOS load device is a PMOS transistor, wherein the source of the PMOS transistor is connected to the power supply voltage and the drain of the PMOS transistor is connected to the amplifying unit wherein the second load device further comprises: a compensation unit which is connected to the negative feedback buffering unit and compensates for both a gain and a frequency characteristics in the high frequency range. The gate of the NMOS transistor of the negative feedback load buffering unit is connected to the drain of the PMOS transistor, the source of the NMOS transistor of the negative feedback load buffering unit is connected to the gate of the PMOS transistor, and the drain of the NMOS transistor is connected to the power supply voltage.

Using an active load PMOS, to replace a passive load resistor can dramatically reduced the required chip area for the circuit while also helping produce much higher gains (due to the potentially high small-signal resistance an active load can provide). An active load can be implemented using a gate-drain connected (a.k.a. diode-connected) MOSFET or a current source/sink. Amplifiers with gate-drain connected active loads tend to achieve large frequency bandwidths but low gain due to their relatively low output impedance. For examples of PMOS amplifiers using gate connected active loads is shown in circuit diagram below.

Circuit Diagram:



Netlist Codes:

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* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on April 23, 2010 at 23:00:15
* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="File1.sdb"
+ probetopmodule="Module0"
* Main circuit: Module0
M1 out in Gnd Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u
M2 out out N5 N5 Ph L=.15u W=.9u AD=66p PD=24u AS=66p PS=24u
v3 in Gnd 5.0
v4 N5 Gnd 5.0
.include "D:\Tanner\Model file\dual.md"
.dc v3 0 5 .1
.print v(in) v(out)
* End of main circuit: Module0
```
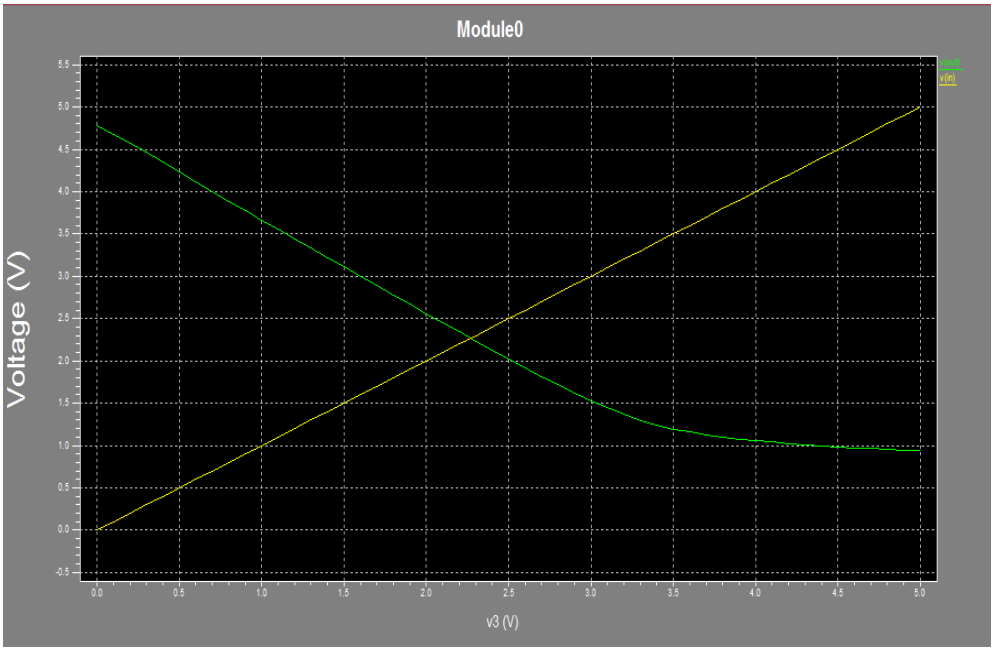

Characteristic Graph:

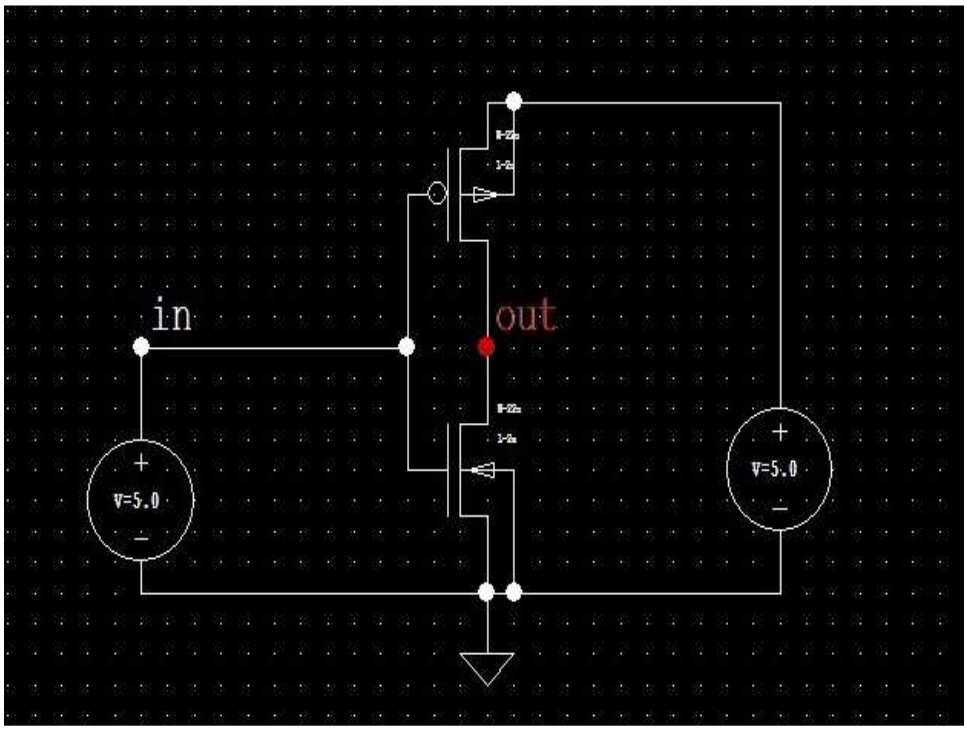


Assignment 3: CMOS Inverter

A CMOS inverter circuit is shown in circuit diagram below It consists of two opposite polarity MOSFETs the NMOS and the PMOS with their gates connected together at the input; the applied voltage is denoted by An NMOS-PMOS group with a common gate is called a complementary pair**,** which gives us the “C” in “CMOS.”, the complementary pair forms the basis for CMOS logic circuits. The inverter output voltage is taken from the common drain terminals. The transistors are connected in a manner that ensures that only one of the MOSFETs conducts when the input is stable at a low or high voltage; this is due to the use of the complementary arrangement.

The DC characteristics of the inverter are portrayed in the voltage transfer characteristic, which is a plot of V_{out} as a function of V_{in}. This is obtained by varying the input voltage V_{in} in the range from 0 to V_{DD} and finding the output voltage V_{out}. The VTC for the circuit is obtained by starting with an input voltage of V_{in} =0v and then increasing it up to a value of $\mathbf{V_{in} = V_{DD}}$. This results in the plot shown in the characteristic graph.

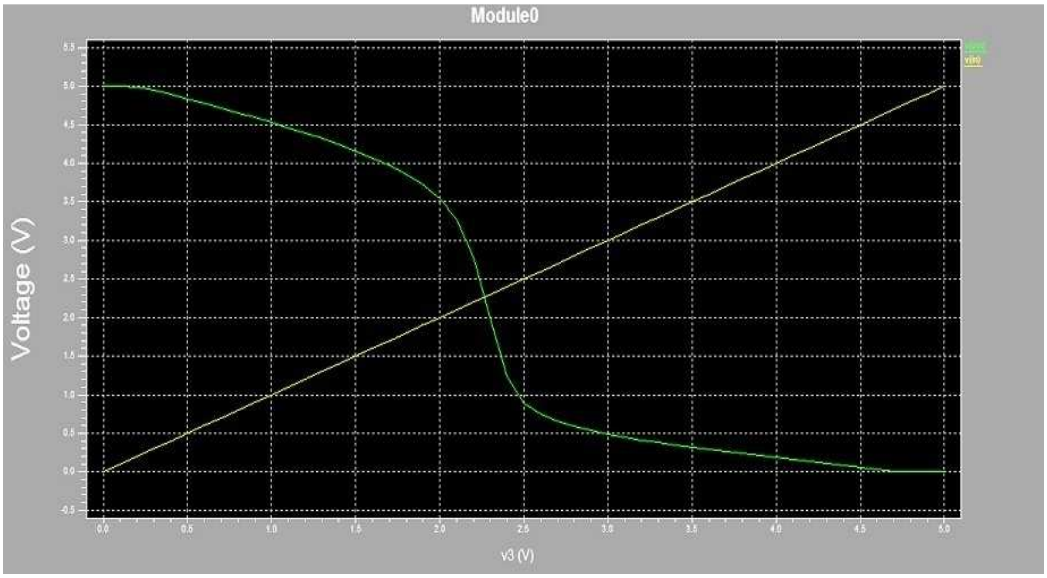
Circuit Diagram:



Netlist Codes:

```
* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on April 26, 2010 at 21:05:43
* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="inv.sdb"
+ probetopmodule="Module0"
* Main circuit: Module0
M1 out in Gnd Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u
M2 out in N2 N2 Ph L=.15u W=.9u AD=66p PD=24u AS=66p PS=24u
.include "N:\Model file\dual.md"
v3 in Gnd 5.0
v4 N2 Gnd 5.0
.dc v3 0 5 .1
.print v(in)v(out)
* End of main circuit: Module0
```

Characteristic Graph:



Assignment 4: Resistive Load Inverter

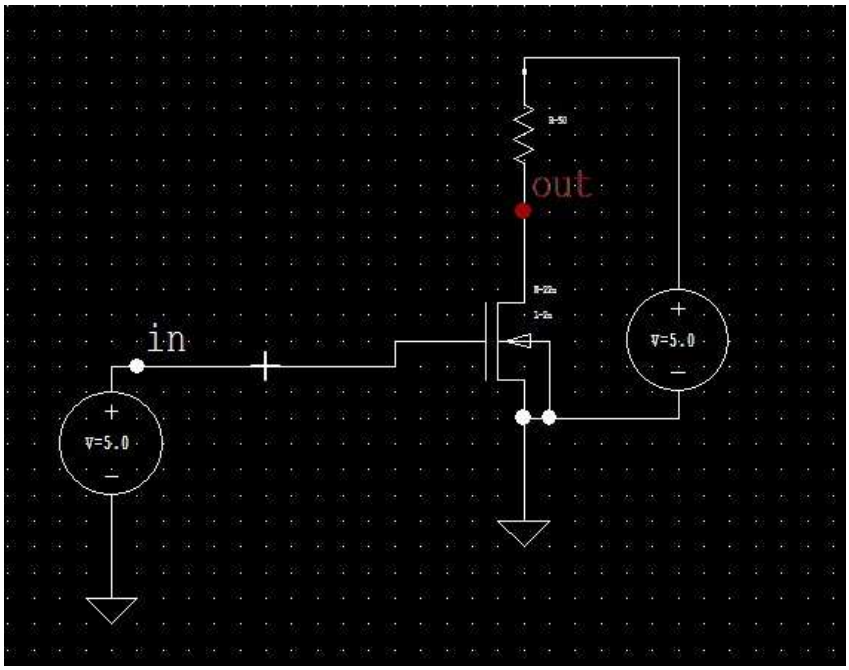
The resistive load is straight forward but unattractive. Circuit resistances in integrated circuits must be implemented using the resistivity of the various conducting regions. This resistivity is usually too low for this to be an economic solution. The inverter consists of a single inverting transistor, together with a load to convert the change in transistor current into the voltage change suitable for the following gates. This arrangement is not often used because of the large space requirements of resistors produced in a silicon substrate. This basic pull down arrangement is shown in figure.

The output voltage when V_{in} is high is given by

$$V_{out} = V_{DD} Z_{on} / Z_{on} + Z_L$$

Where Z_L is the load impedance, The typical values required of Z_L to be at least 4 times of Z_{on} to provide a sufficiently low voltage for subsequent stages. The load required may be implemented by several different mechanisms: resistance, enhancement transistor, depletion transistor and p-channel transistor.

Circuit Diagram:



Netlist Codes:

* SPICE netlist written by S-Edit Win32 Demo 9.12

* Written on April 26, 2010 at 20:49:45

* Waveform probing commands

.probe

.options probe filename="resistive inv.dat"

+ probe sdb file="I:\Users\Sush\Desktop\Tanner EDA\Tanner EDA\Demo\T-Spice\resistive inv.sdb"

+ probe top module="Module0"

* Main circuit: Module0

M1 out in Gnd Gnd NH L=0.15u W=0.45u AD=66p PD=24u AS=66p PS=24u

R2 N3 out 5k TC=0.0, 0.0

v3 N3 Gnd 5.0

v4 in Gnd 5.0

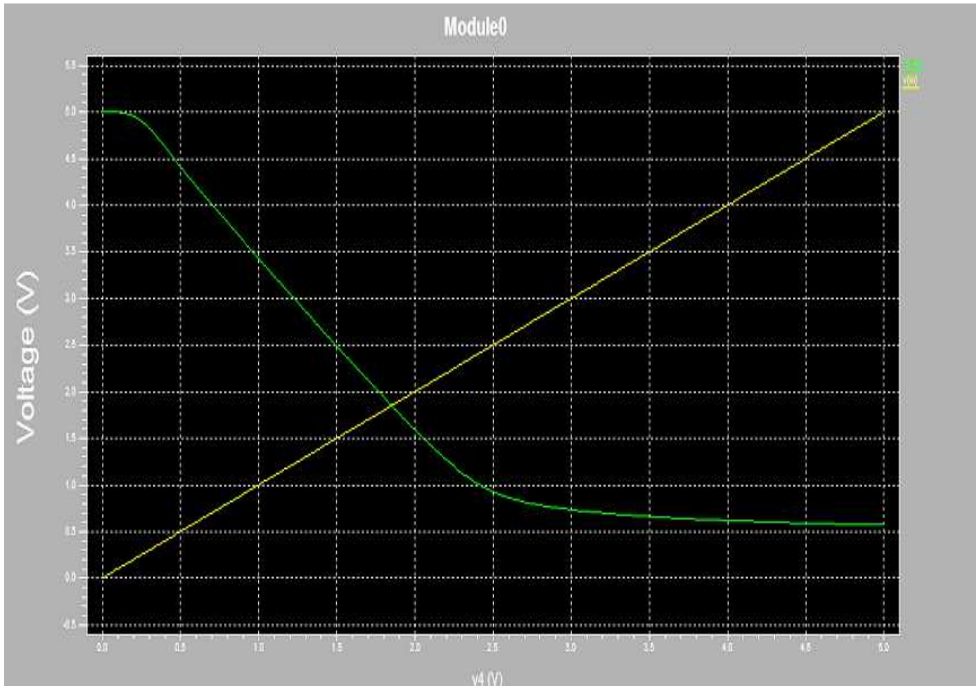
.include "N:\Model file\dual.md"

.dc v4 0 5 .01

.print v(in) v(out)

* End of main circuit: Module0

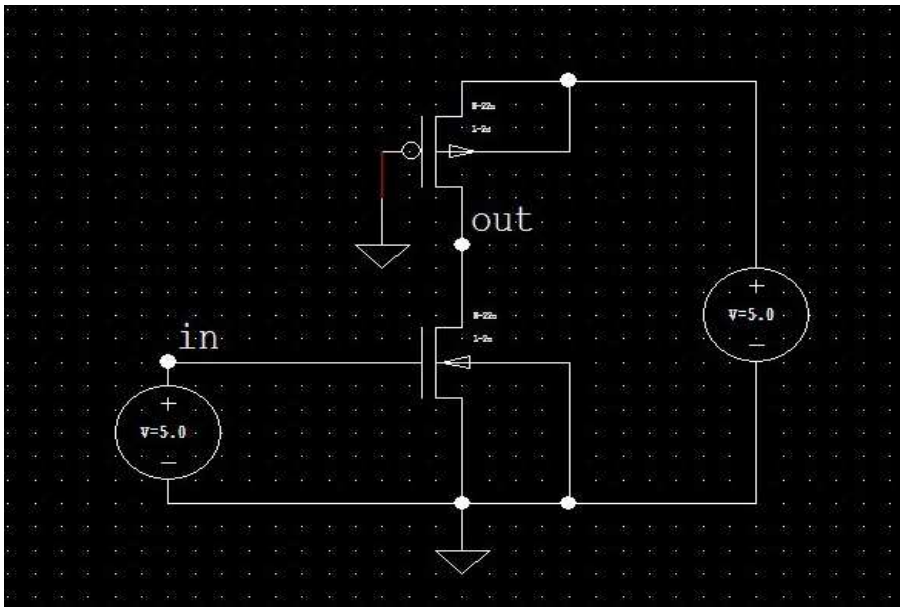
Characteristic Graph:



Assignment 5: Pseudo-NMOS inverter

A pseudo-NMOS logic implemented in a CMOS circuit typically includes a load PMOS with its gate tied to ground (GND), so that the load PMOS is always ON. The source and the drain of the load PMOS are connected between the supply voltage (V_{DD}) and a "pull-down" NMOS tree or circuit, respectively. A typical conventional pseudo-NMOS logic implemented in a CMOS circuit is shown in fig. The pull-down NMOS tree implements the desired equations of the pseudo-NMOS logic. A leakage occurs when there is undesirable current flow from source to drain even when the input voltage to the NMOS is zero or near zero. In other words, the NMOS do not act as a perfect switch. Power differential or noise at the inputs to the NMOS solved the leakage problem, which results in noise being transmitted to other circuits that are connected to the output node of the pseudo-NMOS circuit. The size (i.e., the width) of the load PMOS can be increased to counter input noise and NMOS leakage. In this manner the PMOS becomes stronger (i.e., able to drive more current) so that there is less impact on the PMOS by the leakage. However, this approach undesirably increases the voltage output level when the NMOS are turned ON to produce a logical LOW value at the output. Alternatively, the size of the NMOS can be decreased. The circuit diagram and Characteristic graph is shown below.

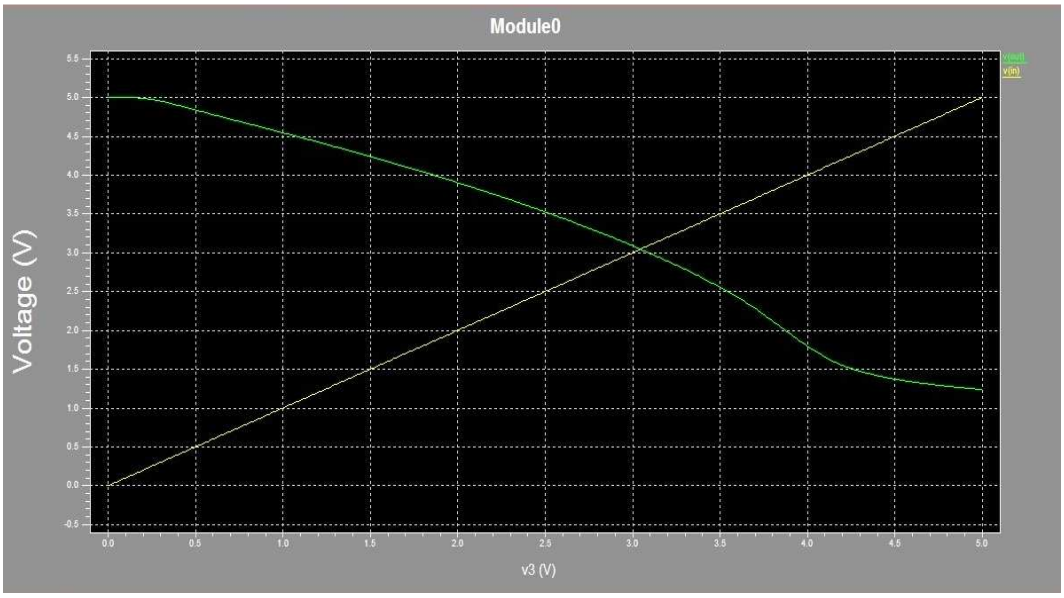
Circuit Diagram:



Netlist Codes:

```
* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on April 26, 2010 at 23:06:39
* Waveform probing commands
.probe
.options probe file name="sedit.dat"
+ probesdb file="File1.sdb"
+ probetopmodule="Module0"
* Main circuit: Module0
M1 out in Gnd Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u
M2 out Gnd N5 N5 Ph L=.15u W=.9u AD=66p PD=24u AS=66p PS=24u
v3 in Gnd 5.0
v4 N5 Gnd 5.0
.include "D:\Tanner\Model file\dual.md"
.dc v3 0 5 .01
.print v(in) v(out)
* End of main circuit: Module0
```

Characteristic graph:



Assignment 6: Dynamic Inverter

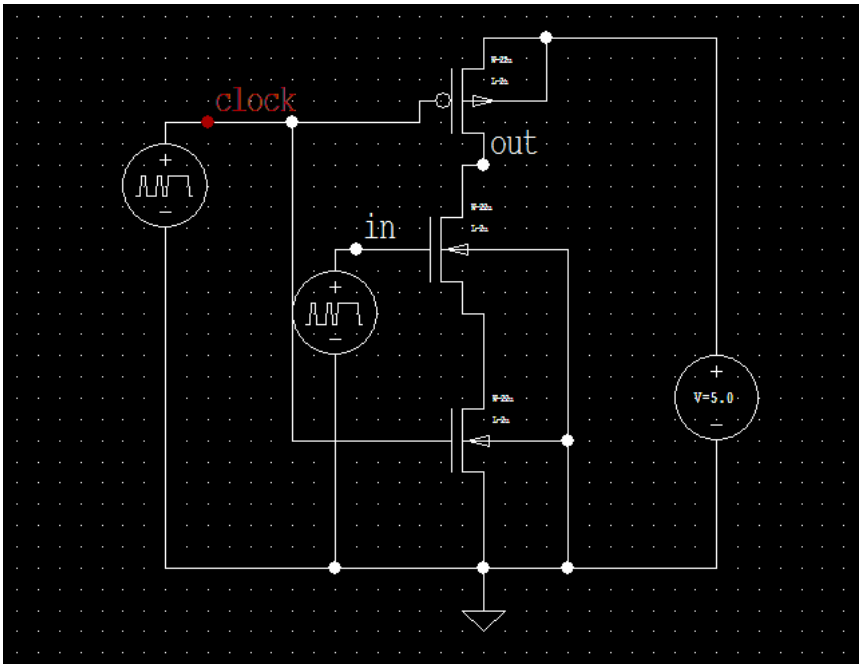
In a dynamic inverter system the charging system operates normally with the inverter off. A regulator inside the inverter controls charging voltage. When the inverter is turned ON the alternator is disconnected from the vehicle battery and tied into a transformer that uses electronic controls to change the DC alternator input to AC inverter output. A separate transformer winding provides battery charging so fully regulated 120 volt AC and 12 volt DC power is available continuously as long as the engine is running above a minimum RPM. Power can be used while the vehicle is being driven although stopping in traffic can result in greatly reduced output.

The inverter delay t_d is determined by the drive current I_{on}, V_{DD}, the non-linear capacitances of the intrinsic transistors, and the interconnect capacitances. The capacitances are modelled into a single load capacitance at the inverter output. The influence of the non-linear capacitances can also be formulated as follows: For switching one transistor a total switching charge of

$$Q_{sw}(V_{DD})=Q_{G,ON}(V_{DD})-Q_{G,OFF}(V_{DD})+Q_{D,OFF}(V_{DD})-Q_{D,ON}(V_{DD})$$

is transferred.

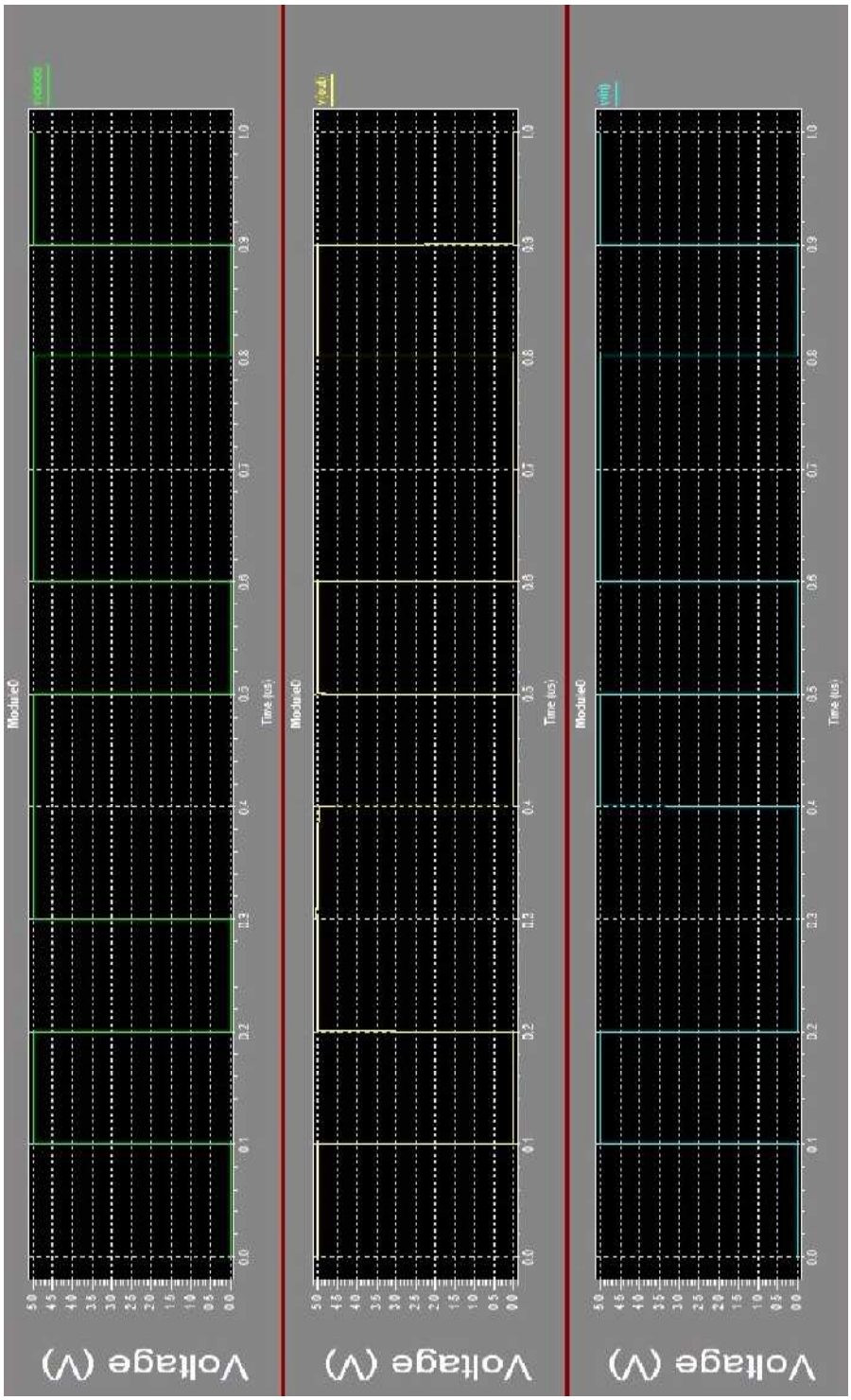
Circuit Diagram:



Netlist Codes:

```
* SPICE netlist written by S-Edit Win32 Demo 9.12

* Written on May 2, 2010 at 23:16:35

* Waveform probing commands

.probe

.options probefilename="File1.dat"

+ probesdbfile="I:\Users\Sush\Desktop\Tanner EDA\Tanner EDA\Demo\T-Spice\File1.sdb"

+ probetopmodule="Module0"

* Main circuit: Module0

M1 N2 clock Gnd Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u

M2 out in N2 Gnd Nh L=.15u W=.45u AD=66p PD=24u AS=66p PS=24u

M3 out clock N1 N1 Ph L=.15u W=.9u AD=66p PD=24u AS=66p PS=24u

v4 clock Gnd bit({01011011} pw=200n on=5.0 off=0.0 rt=.10n ft=.10n delay=0 lt=100n ht=100n)

v5 in Gnd bit({01001011} pw=200n on=5.0 off=0.0 rt=.10n ft=.10n delay=0 lt=100n ht=100n)

v6 N1 Gnd 5.0

.include "D:\Tanner\Model file\dual.md"

.tran .1ns 1000ns

.print v(in) v(out) v(clock)

* End of main circuit: Module0
```

Characteristic graph:



Comparative Study:

An important issue in the design of VLSI circuits is the choice of the basic circuit approach and topology for implementing various logic and arithmetic functions. Here several static and dynamic CMOS circuit design styles are evaluated in terms of area, propagation delay and power dissipation. The different design styles are compared by performing detailed transistor-level simulations on a benchmark circuit using TSPICE, and analysing the results, based on the results of our analysis, some of the trade-offs that are possible during the design phase in order to improve the circuit power-delay product are identified. Power consumption factors such as leakage and device capacitance are inherently dependent on the type of logic family chosen to implement an application which compares the suitability of static CMOS, pseudo-NMOS logic families for use in near threshold supply voltage. Pseudo-NMOS logic also has a restricted voltage swing, but for a different reason: the PMOS ensuring the level high when the path to ground is off is constantly turned on. However when the path to ground is on, the PMOS resistance may be comparable to the PMOS path resistance. This typically yields several undesirable effects: a level low voltage not at ground level, a constant current consumption and PMOS transistors oversized to reduce the resistance of the path to ground. This effect implies larger gate capacitances. Pseudo-PMOS has been proposed by claiming this logic style presents better voltage transfer characteristic at low voltage and lesser transistors per gate hence achieving best PDP (Power Delay Product). However, logic such as pseudo-PMOS yields a high static power which prevents the circuits to achieve minimum energy consumption. And, the benefit of the limited number of transistors is offset by the increase in gate capacitance to reduce the resistance of the path to ground. The increasing demand for low-power VLSI asks, among others, for power efficient logic styles. Performance criteria for logic styles are circuit speed, circuit size, power dissipation, and wiring complexity as well as ease-of-use and generality of gates in cell-based design techniques. Dynamic logic styles are often a good choice for high-speed, but not for low-power circuit implementations due to the high node activity and large clock loads.