Mobility Enhancement using Germanium

(A Project submitted for the Subject Design and Technology of Electronic Devices)

Tezpur University
2009

Submitted By :

Sujit Kumar Nayak
Roll No : ELDT09006

Under the guidance of:
Asst. Prof. S. Sarma

M.Tech ELDT, Deptt of ECE, Tezpur University University
Napam, Tezpur, Sonitpur, Assam

November 2009

Introduction:

Currently, the increase in drive currents for faster switching speeds at lower supply voltages is largely at the expense of an exponentially growing leakage current, which leads to a large standby power dissipation. There is an important need to explore novel channel materials and device structures, which would provide us with high performance nano-scale MOSFETs. Due to their significant transport advantage, high mobility materials are very actively being researched as channel materials for future highly scaled CMOS. However, most high mobility materials also have a significantly smaller band gap compared to Si leading to very high BTBT leakage currents, which may ultimately limit their scalability. The use of heterostructure DGMOSFETs, can significantly reduce the BTBT tunneling leakage and fully exploit the advantage offered by high mobility channel materials, while retaining excellent electrostatic control of the channel.

2.3.3 Transport in Germanium

Germanium and Silicon belong to the same group IV in the periodic table. Some of the physical and electrical properties of Ge (Table.1) along with the band structure are compared with Si. As seen in Fig.1.1, Ge has a lighter transverse effective mass (mt) for electrons and also a lighter effective mass in the heavy hole (mhh) and light hole (mlh) bands compared to Si. The lighter effective mass in Ge could potentially allow us to obtain higher carrier mobility and drive currents in Ge MOSFETs compared to Si MOSFETs.

Properties	Symbols	Ge	Si	Units
Bandgap at 300 K	E_g	0.66	1.12	eV
Breakdown E-field	E_{BD}	$\sim 10^5$	$\sim 3\times10^5$	V/cm
Dielectric permittivity	κ	16.0	11.9	—
Drift mobility (electron)	μ_e	3900	1500	cm^2/V-s
Drift mobility (hole)	μ_h	1900	450	cm^2/V-s
Effective mass (electron longitudinal)	m_{le}^*	1.64	0.98	—
Effective mass (electron transverse)	m_{te}^*	0.082	0.19	—
Effective mass (heavy hole)	m_{hh}^*	0.044	0.16	—
Effective mass (light hole)	m_{lh}^*	0.28	0.49	—
Intrinsic carrier concentration	n_i	2.4×10^{13}	1.45×10^{10}	cm^{-3}
Melting point	—	937	1415	°C
Saturation velocity	v_{sat}	6×10^6	1×10^7	cm/s
Thermal conductivity at 300 K	k_{th}	0.6	1.5	W/cm-°C

Table:1. Physical and electrical properties of Ge compared to Si

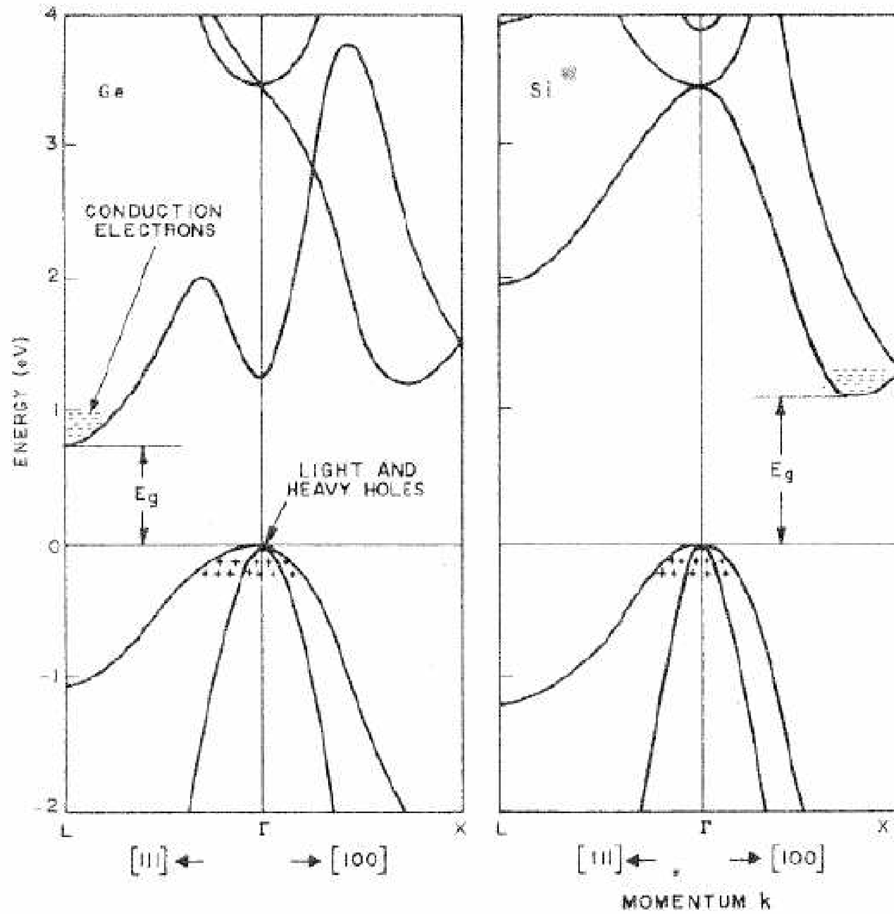

Fig. 1.1. Conduction and Valence band structure of Ge and Si.

As shown in Fig. 1.2 (a) and (b), while the lowest valley for Si is the 6-fold symmetric X-valley along [100], the lowest conduction valley for Ge is the 8-fold symmetric L-valley along [111]. Thus, for both materials, the drive current in MOSFETs will depend strongly on the surface and channel orientation .

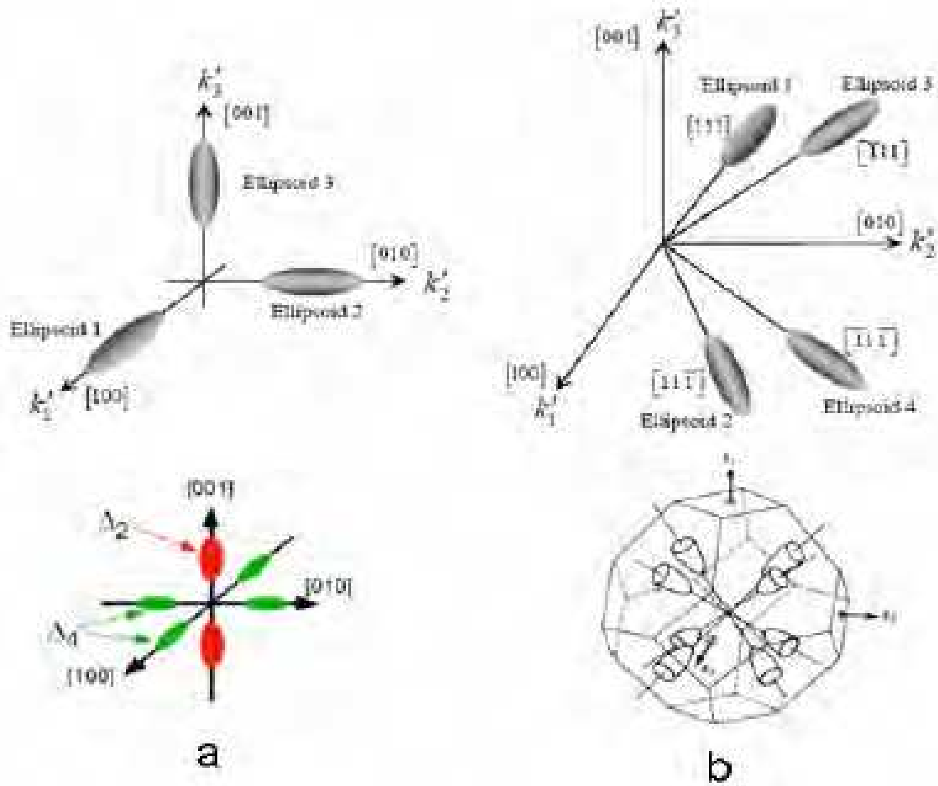

Fig. 1.2 (a). The lowest valley for silicon is 6-fold symmetric and
(b) the lowest valley for germanium is 8-fold symmetric.

Table 2(a) and (b) can be used to extract the effective mass for electrons in MOSFETs fabricated along different crystal orientations for X-valley and L-valley semiconductors.

a

(Wafer)/[transport]/[width]	Valley	m_x	m_y	m_z	Degeneracy
(001)/[100]/[010]	Δ	m_t	m_t	m_l	2
		m_l	m_t	m_t	2
		m_t	m_l		2
	Λ	$m_t \frac{(2m_l+m_t)}{(m_l+2m_t)}$	$\frac{(m_l+2m_t)}{3}$	$\frac{3m_l m_t}{(2m_l+m_t)}$	4
$(111)/[\bar{2}11]/[0\bar{1}1]$	Δ	$\frac{(2m_l+m_t)}{3}$	m_t	$\frac{3m_l m_t}{(2m_l+m_t)}$	2
		$\frac{2}{3}m_t \frac{(2m_l+m_t)}{(m_l+m_t)}$	$\frac{(m_l+m_t)}{2}$	$\frac{3m_l m_t}{(2m_l+m_t)}$	4
	Λ	m_t	m_t	m_l	1
		$\frac{(8m_l+m_t)}{9}$	m_t	$\frac{9m_l m_t}{(8m_l+m_t)}$	1
		$\frac{m_t}{3}\frac{(8m_l+m_t)}{(2m_l+m_t)}$	$\frac{(2m_l+m_t)}{3}$		2
$(110)/[001]/[0\bar{1}0]$	Δ	m_t	$\frac{(m_l+m_t)}{2}$	$\frac{2m_l m_t}{(m_l+m_t)}$	4
		m_l	m_t	m_t	2
	Λ	$\frac{(m_l+2m_t)}{3}$	m_t	$\frac{3m_l m_t}{(m_l+2m_t)}$	2
		$\frac{3m_l m_t}{(2m_l+m_t)}$	$\frac{(2m_l+m_t)}{3}$	m_t	2

b

Material	Valley	m_l	m_t
Silicon	Δ	0.91	0.19
	Λ	1.7	0.12
Germanium	Δ	0.95	0.2
	Λ	1.64	0.08

Table 2.(a) and (b) Effective mass of electrons in different valleys for different surface and channel orientations.

From ballistic transport simulations it has been found that due to their higher injection velocity, Si (100) and Ge (111) provide the highest drive currents at the same inversion charge (Fig. 1.3). Even under ballistic transport conditions, Ge (111) can provide 60% higher drive current than Si (100). Further, due to strong quantum confinement effects (either due to high E-fields in bulk MOSFETs or thinner body thicknesses in FD-SOI/GOI structures), the valley population can change and modify the injection velocity as well as the drive current.

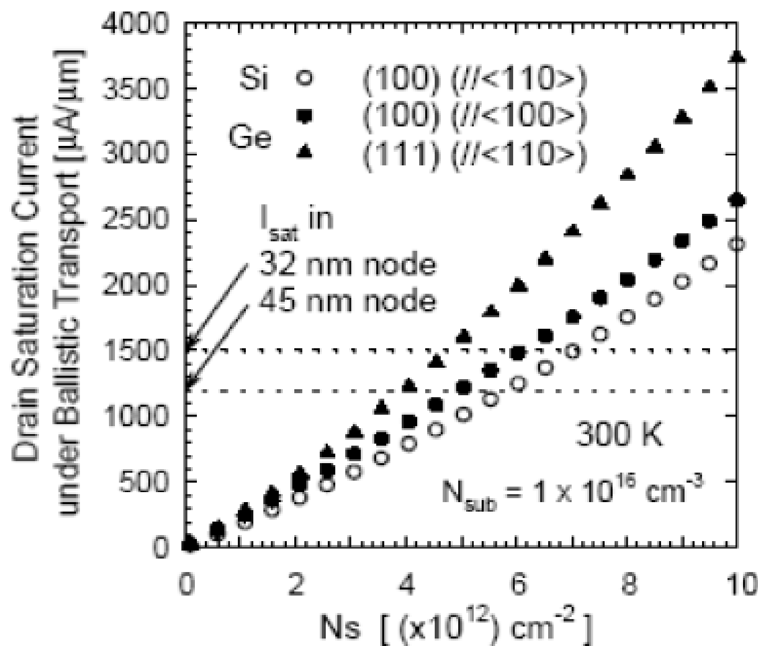

Fig. 1.3. Drain saturation current of Si MOSFETs on (100) surface andGe MOSFETs on (100) and (111) surfaces as a function of NS.

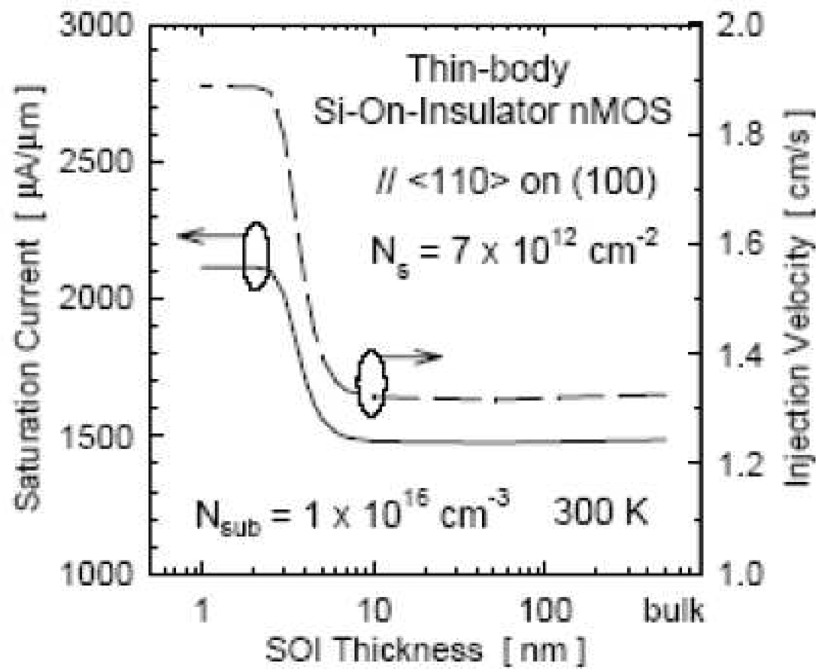

Fig. 1.4. Saturation current as a function of TSOI.

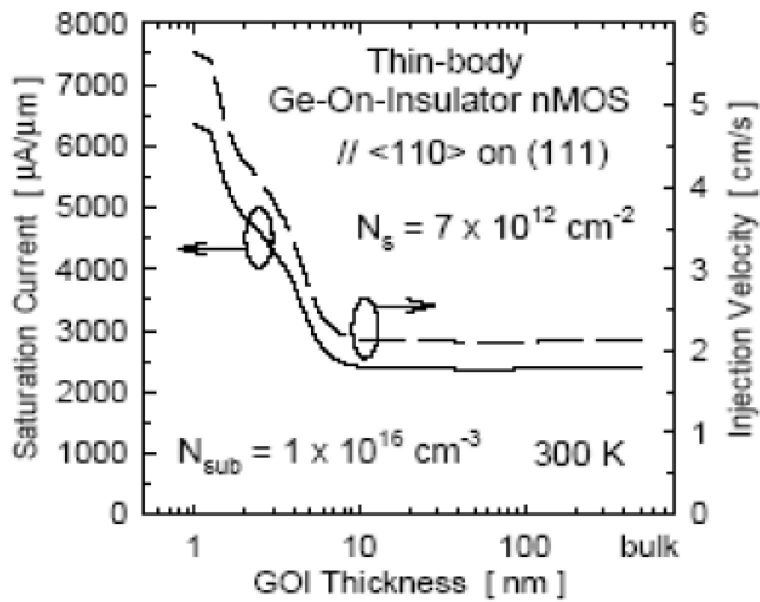

Fig. 1.5. Saturation current as a function of TGOI.

As seen from Fig. 1.4 and Fig. 1.5, for a constant inversion charge, as we go to thinner T-SOI/GOI thicknesses, an enhancement of 42% can be obtained for TSOI<3nm and 160% for TGOI<1nm. This can be easily understood in terms of the increased occupancy of the lowest sub-band, which has the lowest transport effective mass leading to a higher injection velocity (Fig. 1.6). The assumption of constant inversion charge is a big one. The quantum capacitance due to the reduced density of states needs to be taken into account. To evaluate the drive current enhancement, we would like to compare devices at a fixed leakage current and supply voltage.

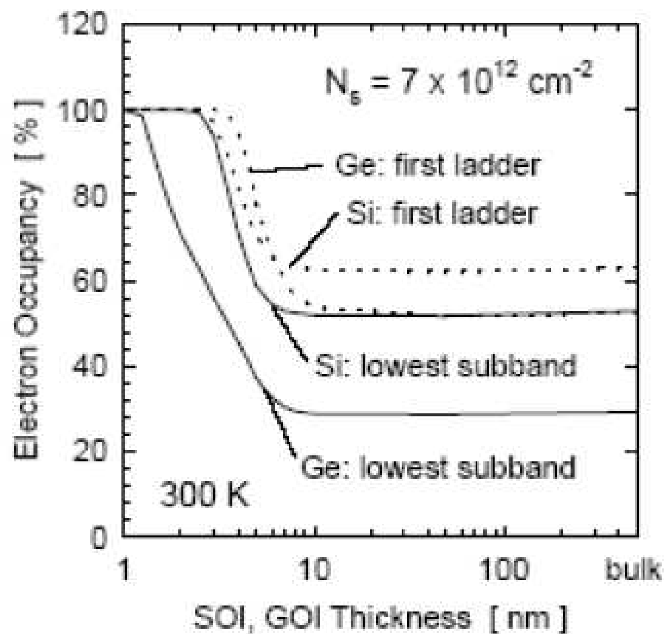

Fig. 1.6. Electron occupancy of the 1st ladder and lowest sub-band as a function of TSOI and TGOI.

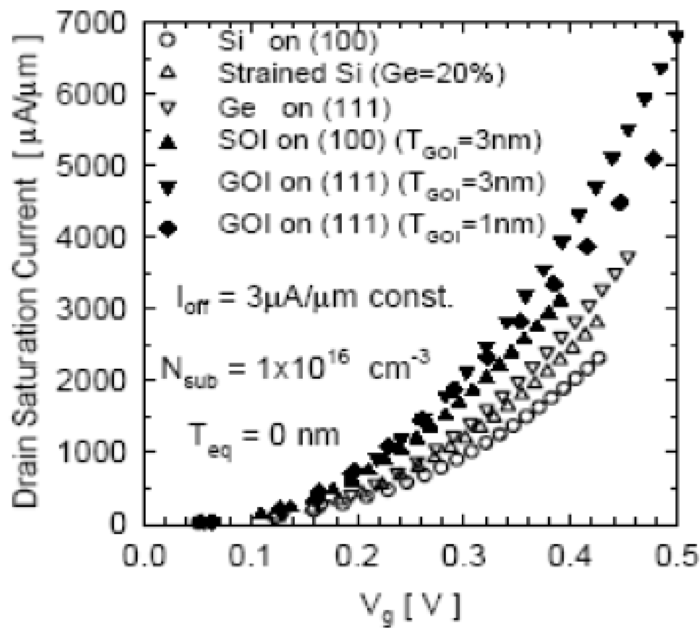

Fig. 1.7. Ultimate Isat-Vg characteristics in the limit of zero nm EOT.

Fig. 1.7 shows the Id-Vg characteristics for the different materials and orientations in the ultimate limit of zero EOT. In this extreme situation, the gate capacitance (and consequently, the inversion charge) is determined entirely by the quantum capacitance.

In this situation, Ge (111) with a TGOI of 3nm shows the highest drive current due to the best tradeoff between injection velocity and quantum capacitance.

Though several theoretical calculations predict a significant enhancement in the electron mobility in Ge n-MOSFETs, most recent experimental results have reported a very poor Ge n-MOS performance (Fig. 1.8).

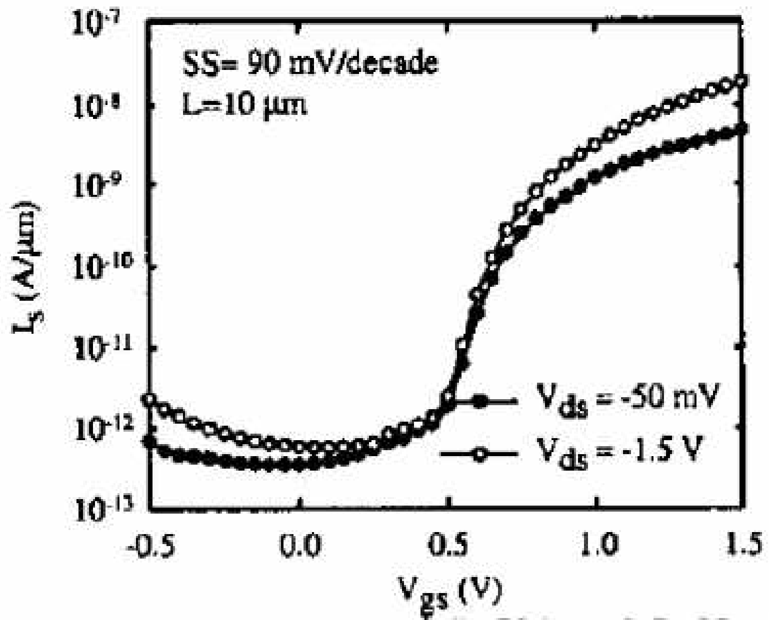

Fig. 1.8. Typical Is-Vg characteristics for Ge n-MOSFETs, reflecting the poor drive currents obtained experimentally.

Since there is no stable high quality native oxide on Ge, the poor performance of Ge n-MOS is usually attributed to practical and technological challenges, primarily concerning the poor Ge high-k insulator interface.

High Mobility, Ultra Thin (UT), Strained Ge MOSFETs on Bulk and SOI with Low Band-To-Band Tunneling (BTBT) Leakage.

Introduction

High mobility channel materials like strained-Ge, Ge and strained Si(x) Ge(1-x) are very promising as future channel materials. However, most high mobility materials also have a significantly smaller band gap compared to Si and suffer from higher BTBT leakage, which may ultimately limit their scalability.

High Mobility, Low BTBT, Ultra-thin, Strained Ge On Bulk Si

Device Structure

Fig. 2.1(a) and (b) show the schematic of the device structure fabricated along with the band structure. Strained Ge is epitaxially grown on lightly doped n-type bulk Si substrate and capped with a thin Si layer. The Si cap was then oxidized at a relatively lower temperature (8000C) to prevent relaxation of the strained Ge film. As Ge can rapidly diffuse from the high Ge % regions into the Si, lowering the Ge%, increasing the Ge pile up at the SiO2 interface and creating defects due to relaxation of the film. The Ge out-diffusion is much faster from the high Ge % region than from the low Ge % region. The effects of the Ge pile up on the interface state density (Dit) and C-Vs measured on MOS capacitors are shown in Figs. 2.2

(a)-(c). The interface state density (Dit) created by the Ge diffusion to the interface is a strong function of TSi cap and can adversely affect the mobility and the trap-assisted-tunneling (TAT).

The different design splits are shown in Table. 2.1.

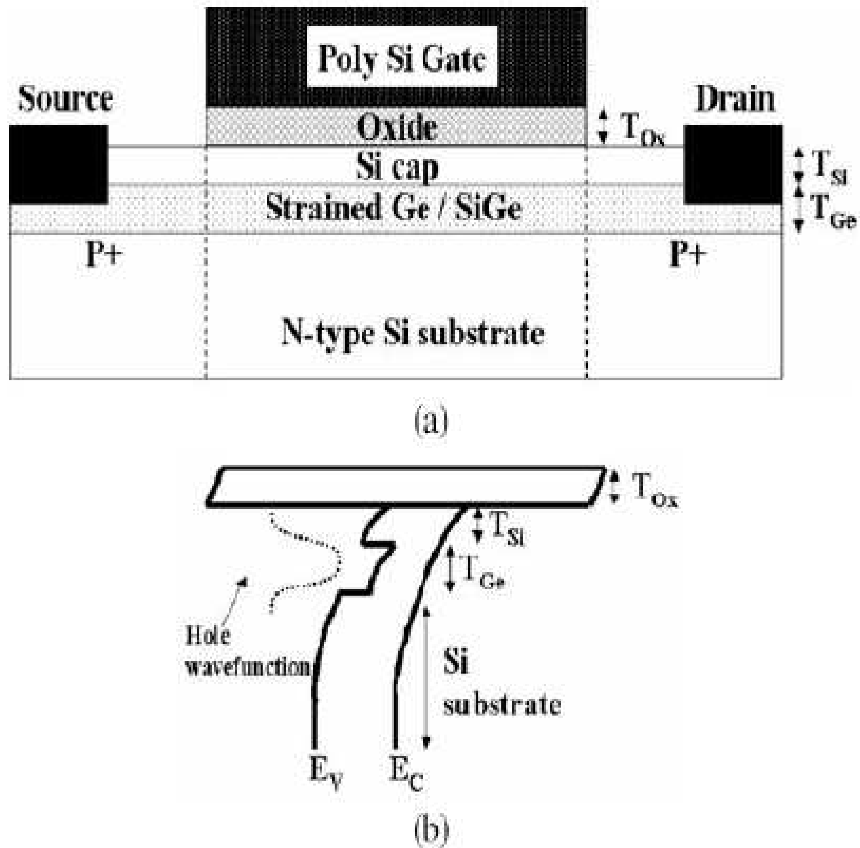

Fig. 2.1. Device structure and band diagrams.

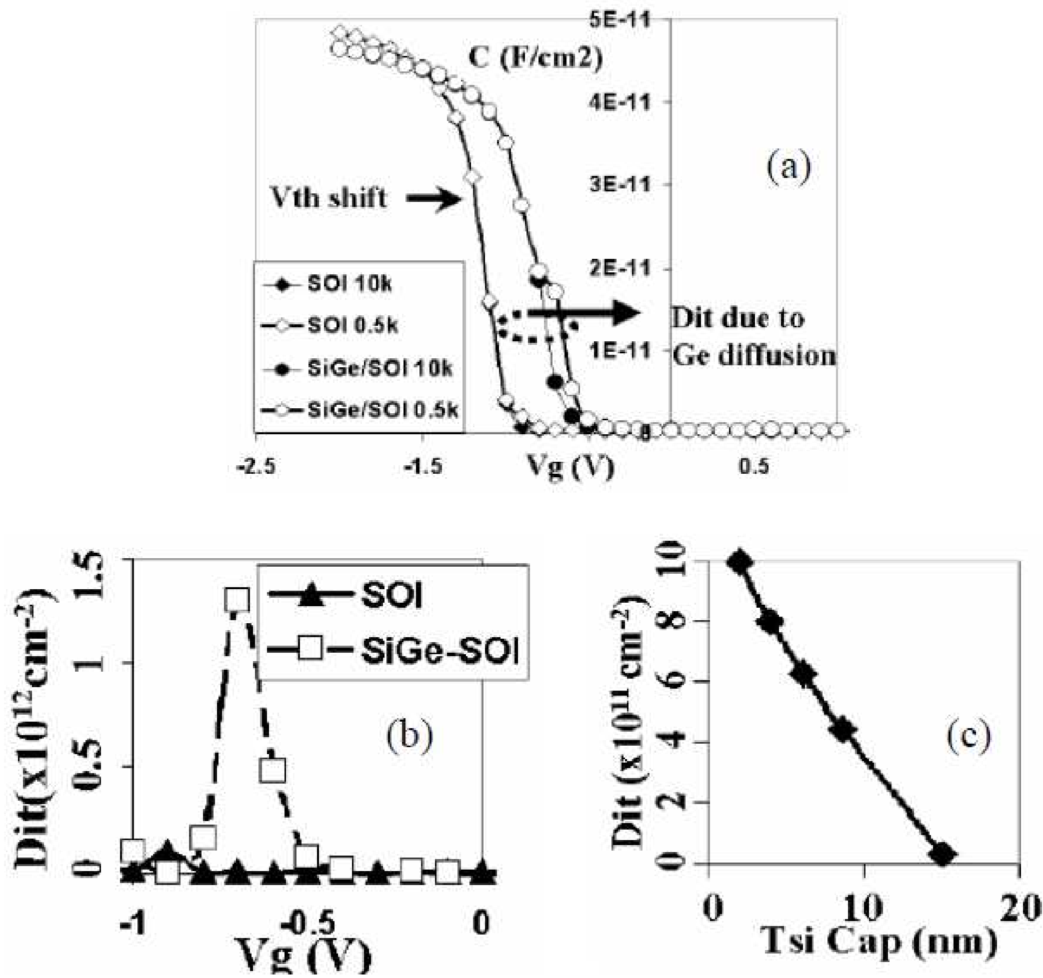

Fig. 2.2. (a)-(c) Interface states and defects generated as a result of Ge diffusion toward the surface are a strong function of the TSi, cap for a given gate oxidation condition.

Mobility Enhancements And Low Tunneling Leakage

From the C-Vs of some of the typical MOSFETs (Fig. 2.3) we can clearly observe a decrease in the Vth due to the band offset between control Si and strained-Ge. Further, we also observe the characteristic

hump in the C-V curve showing the onset of inversion in the Si cap (4nm). Since the 4nm strained Ge layer is close to the critical thickness, it partially relaxes during the gate oxidation leading to defect formation in the Ge channel and Si cap. As seen in Fig. 2.4, due to the larger out-diffusion to the interface and strain-relaxation, the sub-threshold slope for the 4nm strained Ge device is slightly higher (~90mV/dec) compared to the 2nm strained Ge (~68mV/dec) and the Si control (~65mV/dec). The 2nm strained Ge device shows excellent sub-threshold slope due to the ultra-thin channel, which remains fully strained and defect-free. Due to the lower thermal budget, there is also very little Ge pile up at the interface leading to very low Dit. To study the effect of the TSi cap on the mobility, a comparison between devices #1, #2, #3 and #4 is done where TSi cap is varied from 0nm (surface channel) to 8nm on a 6nm, 50%, strained-SiGe epi layer. The mobility enhancement for these devices is around 65% compared to the control Si (Fig. 2.5). Decreasing TSi cap leads to lower mobility at low Ninv because of Coulombic scattering by the increased interface states. As the thickness of the cap increases, the overall mobility reduces due to a greater fraction of the hole populating the Si surface compared to the Ge buried channel. Again, increasing the TSi cap beyond 4nm reduces the BTBT by >10X (Fig. 2.6)

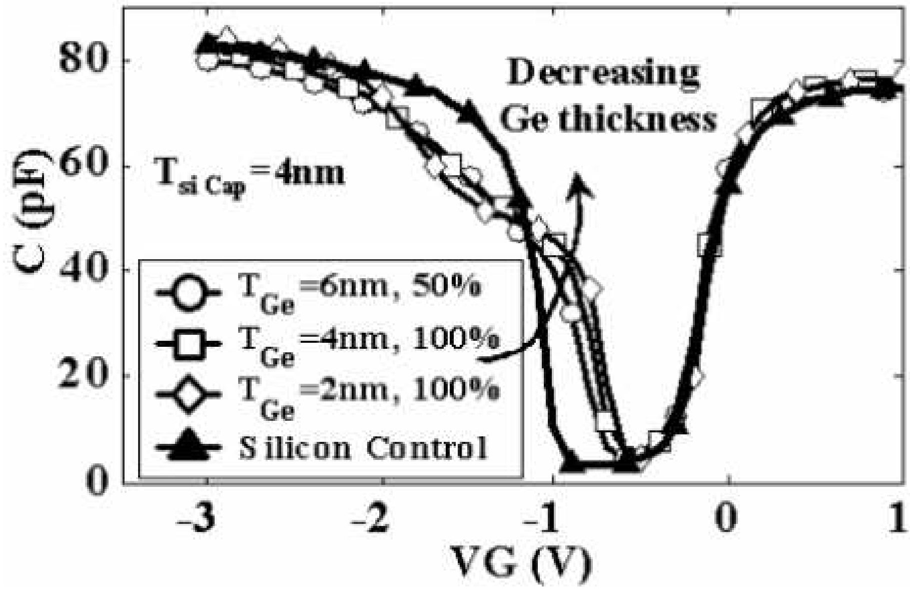

Fig.2.3.C-V for the strained Ge (on bulk Si) channel devices.

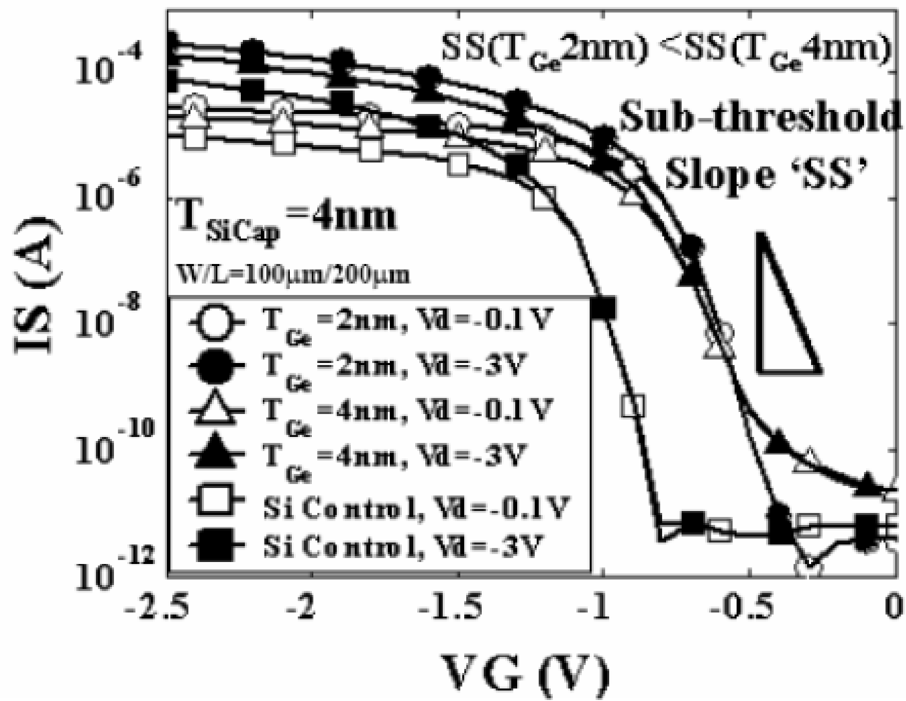

Fig. 2.4. Is-Vg for the strained Ge (on bulk) devices.

Device	$T_{Ge\ Channel}$	Ge %	$T_{Si\ Cap}$
1	6nm	50%	0nm
2	6nm	50%	4nm
3	6nm	50%	6nm
4	6nm	50%	8nm
5	4nm	100%	4nm
6	**2nm**	**100%**	**4nm**
7	Silicon Control		

Table 2.1. Splits for the devices fabricated on bulk substrates.

Simulations show that this is because the Efield in the smaller bandgap, strained-Ge, is decreased by over 50% compared to the surface channel device. The E-field in the Si cap is also slightly lower than the bulk Si control (Fig. 2.7). Thus, as shown in Fig. 2.8, there exists an optimum TSi cap of around 4-6nm, which trades off mobility for BTBT. To see the effect of TGe and Ge fraction on the mobility and BTBT, a comparison of devices #2, #5 and #6 gives that the mobility for the 2nm Ge is much higher (~2X) than the 4nm and 6nm cases. This is because the thicker layers tend to partially relax easily, which releases the strain and causes defects in the channel. The peak mobility for the 2nm case is >3.5X compared to the bulk Si control (Fig. 2.9). Also, the BTBT for the ultra-thin, 2nm, strained Ge is ~10X lower than the thicker Ge case (Fig. 2.10).

The reason for this is two-fold (Fig. 2.11). The first effect is the increase in the effective bandgap of the strained-Ge as we TGe reduces, due to quantum mechanical confinement between the two Si barriers. This higher effective bandgap decreases the probability for BTBT to occur and

reduces the leakage. The second effect is the stronger immunity to partial relaxation of the strain in the film as TGe is decreased.

This relaxation produces defects, which allow trap-assisted tunneling to increase significantly. Thus, from Fig. 2.12, it is found that using ultra thin (2nm), fully strained Ge can help to significantly reduce the BTBT while retaining higher mobility (>3.5X).

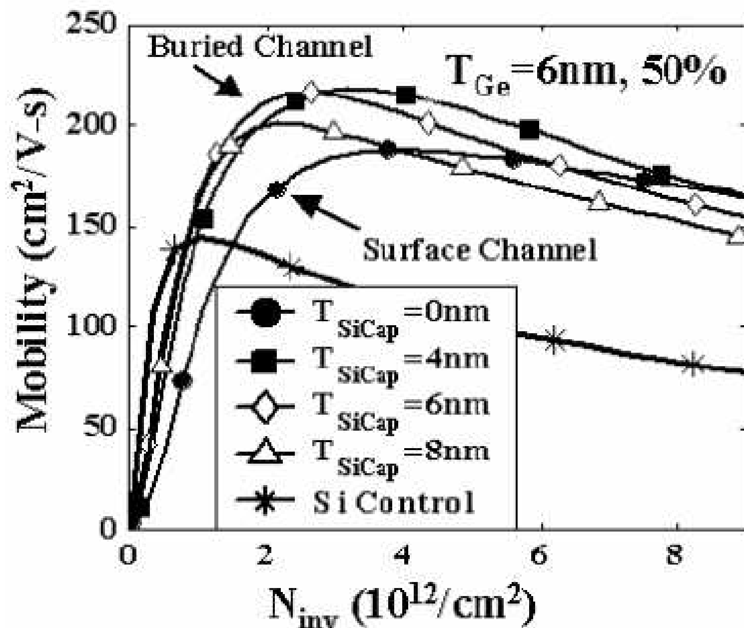

Fig. 2.5. Mobility versus Ninv with varying TSi, cap

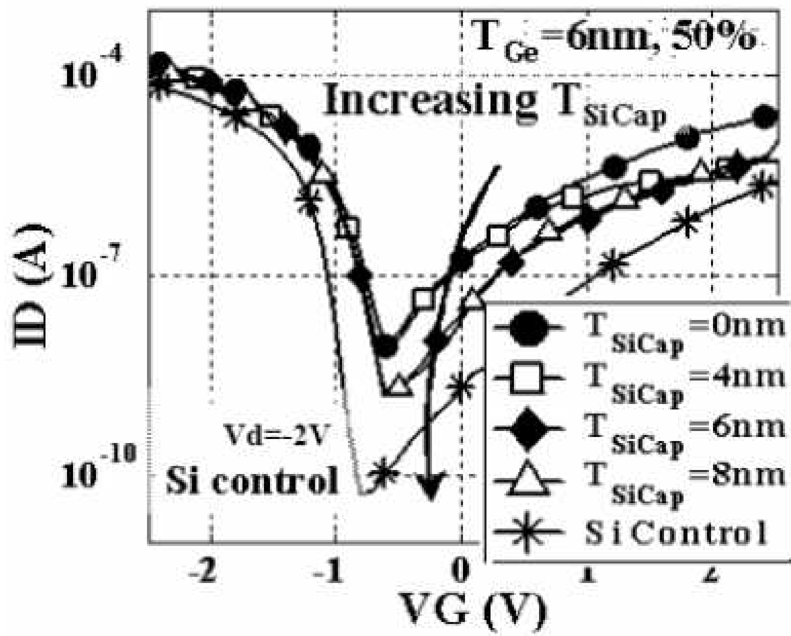

Fig. 2.6. BTBT (gate induced drain leakage, GIDL) with varying TSi, cap

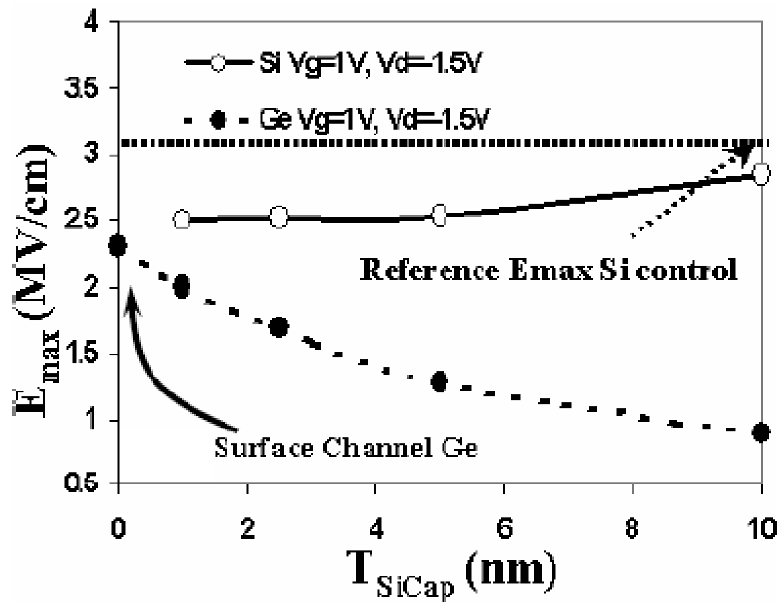

Fig. 2.7. Maximum E-field in the Si cap and Ge channel

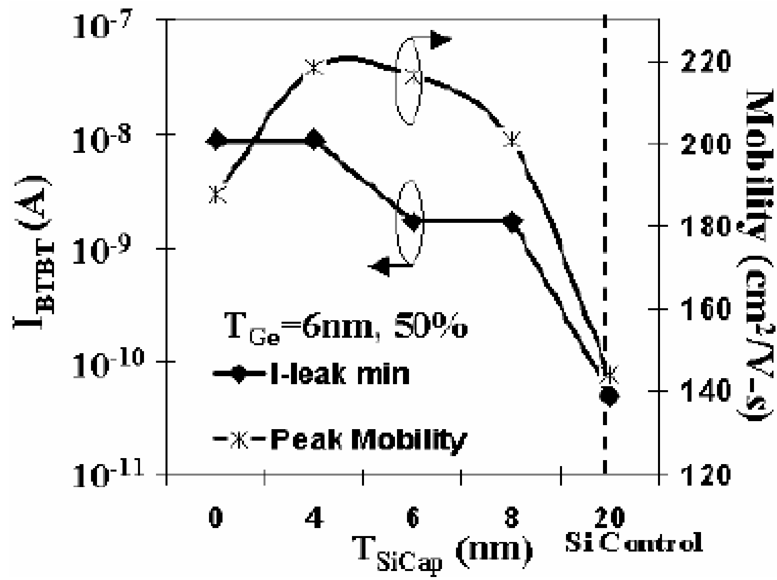

Fig. 2.8. Mobility and BTBT versus TSi, cap

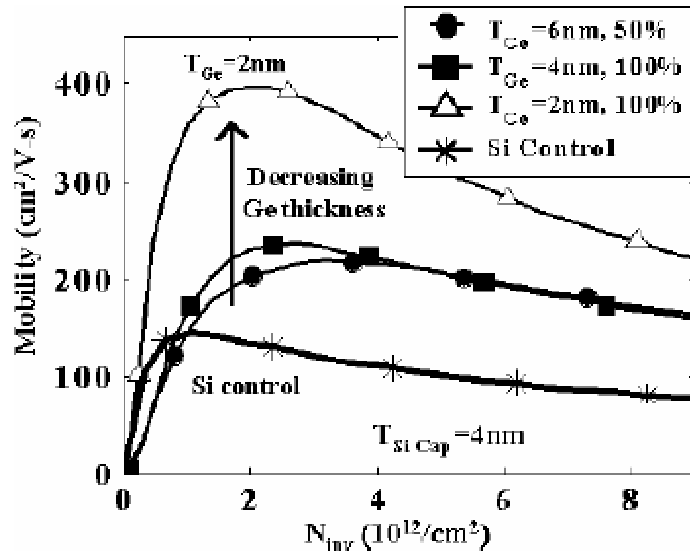

Fig. 2.9. Mobility versus Ninv with varying TGe channel

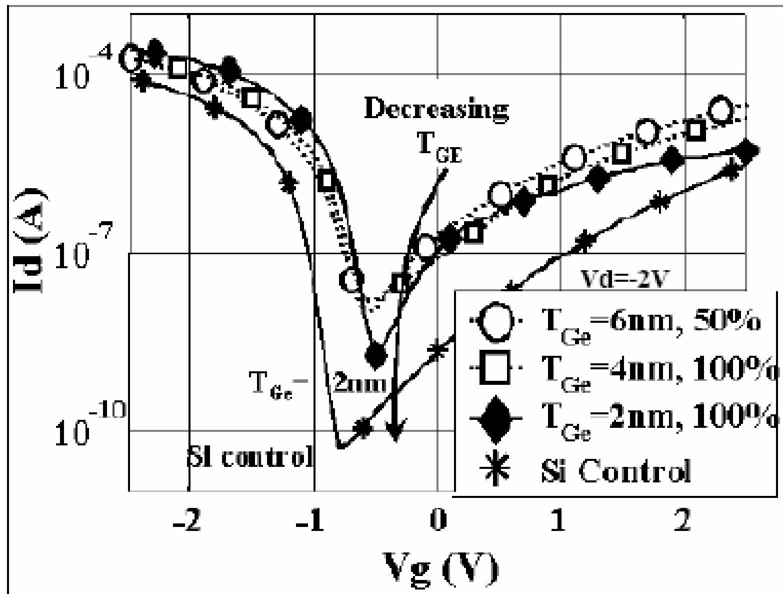

Fig. 2.10. BTBT (GIDL) with varying TGe channel

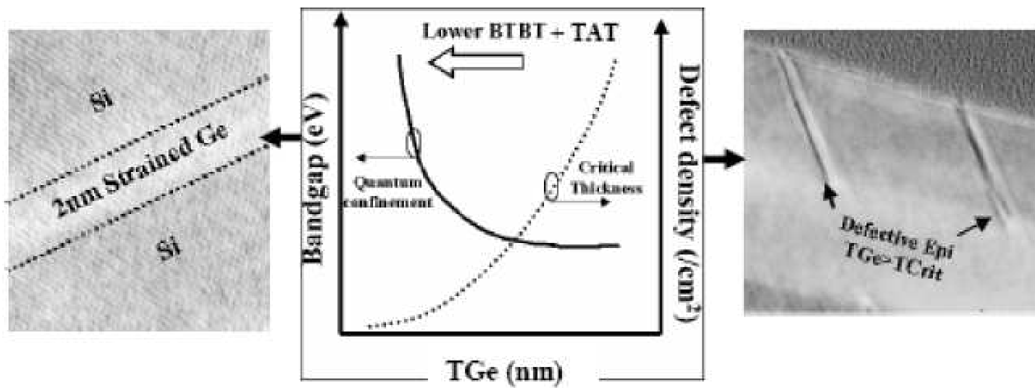

Fig. 2.11. Factors affecting BTBT and TAT

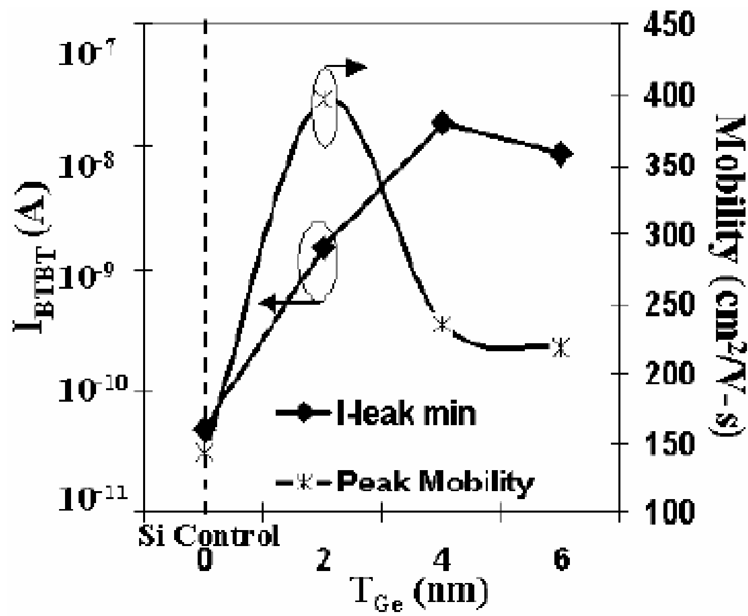

Fig. 2.12. Mobility and BTBT versus TGe channel showing that 2nm is optimum for 100% strained Ge on bulk Si.

Referrences:

1. Tejas Krishnamohan, "Physics And Technology Of High Mobility, Strained Germanium Channel, Heterostructure Mosfets" June 2006.